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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/708,762	03/24/2004	Ming-Jing HO	NAUP0567USA	2761

27765 7590 02/28/2008

NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
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EXAMINER	
SHINGLETON, MICHAEL B	

ART UNIT	PAPER NUMBER
2815	

NOTIFICATION DATE	DELIVERY MODE
02/28/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

winstonhsu.uspto@gmail.com
Patent.admin.uspto.Rcv@naipo.com
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Office Action Summary	Application No.	Applicant(s)	
	10/708,762	HO, MING-JING	
	Examiner	Art Unit	
	Michael B. Shingleton	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4-29-07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 7, 11 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eldridge et al. US 2001/0020743 (Eldridge) in view of either Chittipeddi et al. 5,965,903 or Chittipeddi et al. 6,136,620 both of record and referred to collectively as just "CHITTIPEDDI '903 AND '620" in the text of this rejection.

FIG. 1

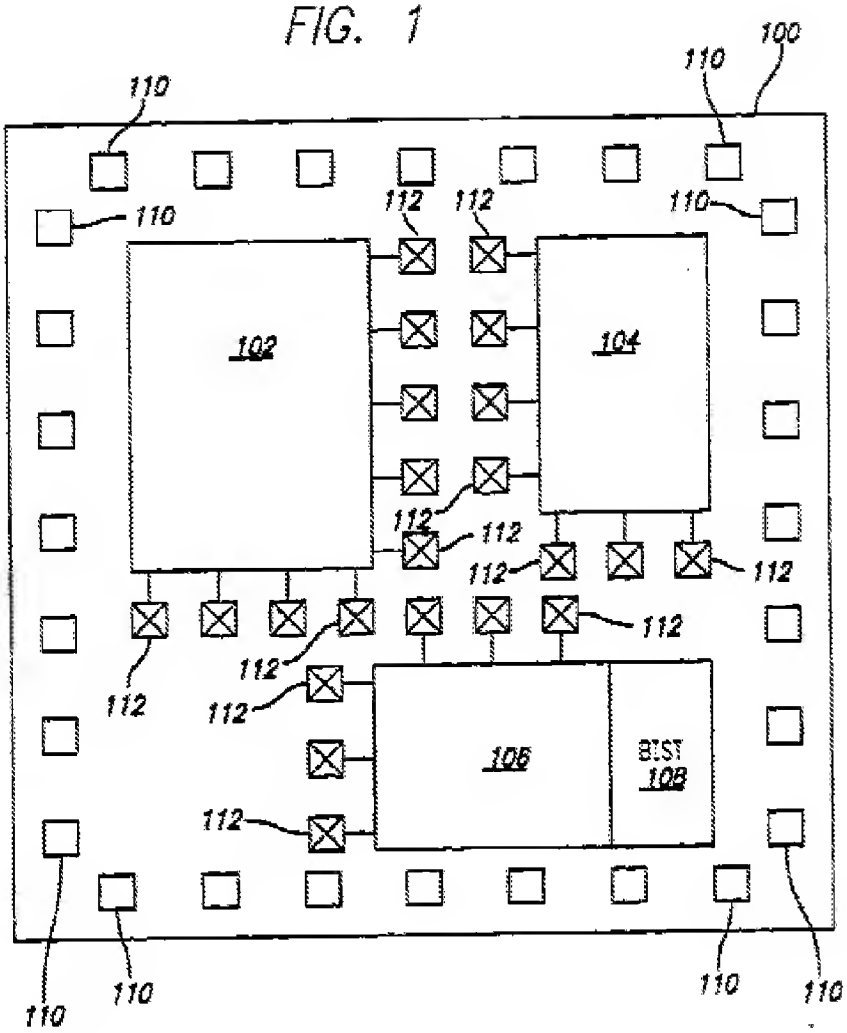

Figure 1 of Eldridge.

Figure 1 and the relevant text of Eldridge discloses the basic structure that makes up applicant's claimed invention which includes an embedded memory circuit with the associated logic elements (See paragraph 0043.), a BIST 108 and a plurality of bonding pads that are formed around or near the entire edge of the chip 100. Eldridge has the BIST circuit in the main circuit area instead of under the bonding pads as is claimed. As to the statements on how applicant intends to use the BIST these statements do not

identify any structure and are as stated merely statements of intended use. Clearly, the Eldridge would be capable of being used this way.

CHITTIPEDDI '903 AND '620 discloses that it is well known to form the BIST circuitry under the bonding pads so as to save space, etc.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to move the BIST circuitry of Eldridge under the bonding pads 110 so as to save space as taught by CHITTIPEDDI '903 AND '620.

Claims 2 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eldridge et al. US 2001/0020743 (Eldridge) in view of either Chittipeddi et al. 5,965,903 or Chittipeddi et al. 6,136,620 both of record and referred to collectively as just "CHITTIPEDDI '903 AND '620" in the text of this rejection as applied to claims 1, 7, 11 and 17 above, and further in view of Lee et al. US 2002/0113287 (LEE '287).

Eldridge is silent on there being Vdd and Vss power rails that are formed under the bonding pads wherein these power supply rails then "encircles" the center area of the IC.

Fig. 2

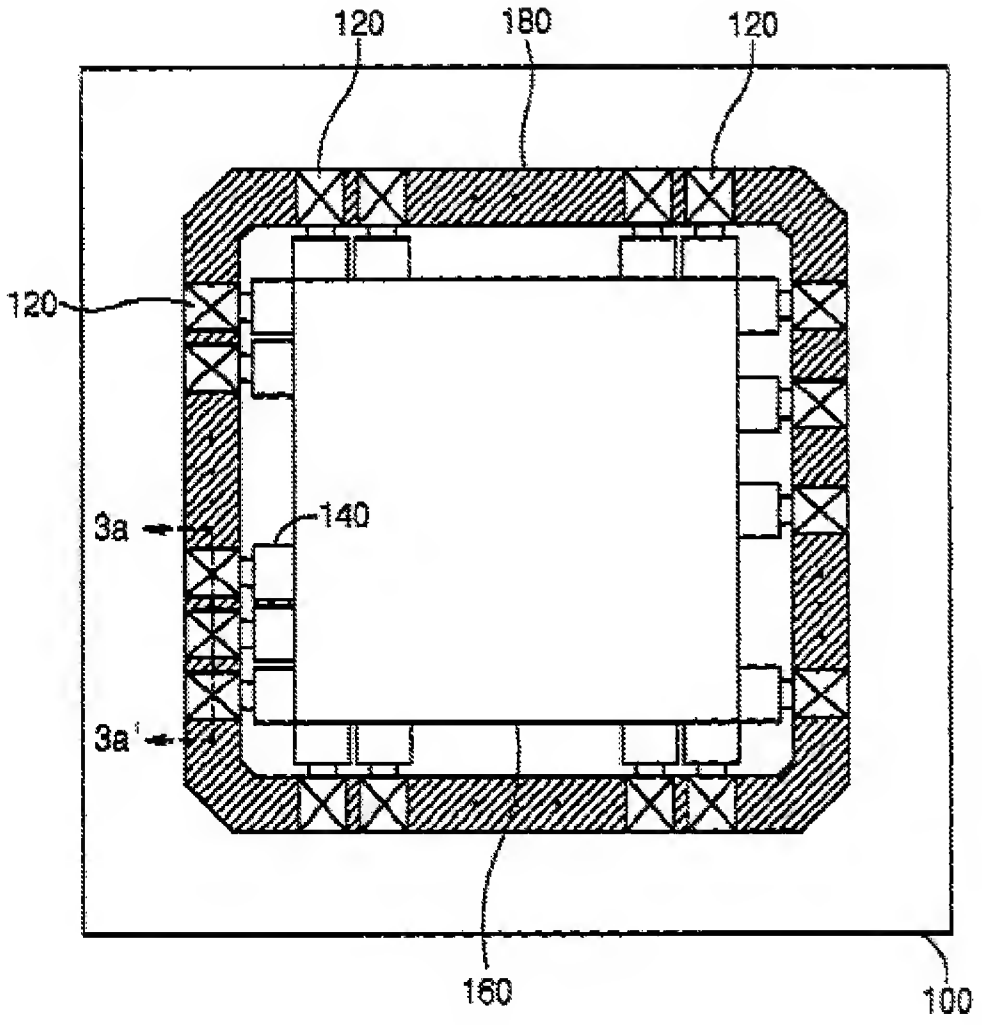

Figure 2 of Lee ‘287

Fig. 4

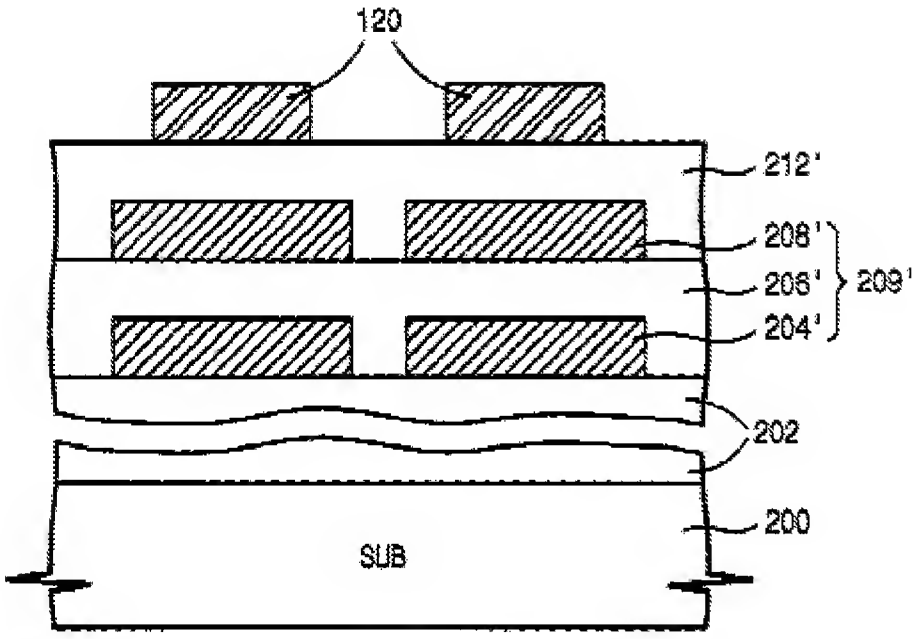

Figure 4 of Lee '287.

LEE '287 teaches that it is well know to form both the power supply rails 204 and 208 under the bonding pads 120 which saves space.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the power supply rails under the bonding pads so as to completely encircle the center circuit area and save space as compared to a structure that employs the power supply rails within the center circuit area as taught by Lee '287.

Claims 3-6, 8-10, 13-16, and 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eldridge et al. US 2001/0020743 (Eldridge) in view of either Chittipeddi et al. 5,965,903 or Chittipeddi et al. 6,136,620 both of record and referred to collectively as just "CHITTIPEDDI '903 AND '620" in the text of this rejection as applied to claims 1, 7, 11 and 17 above, and further in view of Lee et al. US 6,298,001 of record (LEE '001).

LEE '001 teaches that FET switches can be used to switch on an off the power to a circuit within an IC.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a switch like a FET or the like to connect the power supply to a circuit such as the BIST in Eldridge so as to control the turning on and off of this internal circuit as taught by Lee '001. This of course will save power when such a circuit is not needed and thus also reduce thermal effects of the circuit when it is in operation as is clearly evident to those of ordinary skill upon reading the Lee '001 reference.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael B. Shingleton whose telephone number is (571) 272-1770.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker, can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Michael B. Shingleton/

MBS
February 8, 2008

Michael B Shingleton
Primary Examiner
Group Art Unit 2815